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13th Workshop on Crystalline Silicon Solar Cell Materials and Processes

Summary Discussion

Bhushan Sopori, Editor

Prepared by:
R. Sinton, T. Tan, D. Swanson, and B. Sopori

Workshop held at Vail Marriott Mountain Resort
Vail, Colorado
August 10-13, 2003

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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Executive Summary

The 13th Workshop on Silicon Solar Cell Materials and Processes was held in Vail, Colorado, on August 10-13, 2003. The workshop was attended by 109 scientists and engineers from 22 international PV and semiconductor companies, and 22 research institutions from many different countries. A combination of oral, poster, and discussion sessions appraised recent advances in crystal growth, new cell structures, new processes and process-characterization techniques, and cell-fabrication approaches suitable for future manufacturing demands. This year's theme, "Meeting the Challenges of c-Si Photovoltaics," was selected to emphasize new challenges associated with increasing PV production and the introduction of new technologies to lower PV energy costs.

The discussion sessions addressed recent progress, critical issues in implementing new technologies, and the role of fundamental R&D in the growing PV industry. For the first time, we included a rump session, which was held on Sunday evening, August 10th. This session included a panel of representatives, from various photovoltaic companies, who led a discussion of "R&D Challenges in Si PV."

A special poster/presentation session was held on Monday evening, in which NREL/DOE subcontractors highlighted their results of research performed during the current subcontract period. This session served as a subcontract review.

The workshop offered special sessions to discuss: (1) High-Efficiency Si Solar Cells, which reviewed progress made in implementing high-efficiency Si solar cell fabrication processes in the manufacturing environment; (2) Advanced Processing, as future potential approaches for making Si solar cells; (3) Commercial Issues, which addressed basic understanding behind recent processes that have been used by the PV industry, and (4) Automation and Equipment, to address capabilities and requirements of new manufacturing equipment.

Graduate Student Awards were giving to 9 students representing Georgia Institute of Technology, North Carolina State University, University of California-Berkeley, Texas Tech University, Massachusetts Institute of Technology, University of Northern Colorado, and IMEC for their research work in photovoltaics. Each student received a $250 check from funds contributed by the PV industry.

Rump Session: R&D Challenges in Si-PV

Moderator: B. L. Sopori, NREL

Panelists: T. Bruton, BP Solar
J. Hanoka, Evergreen Solar, Inc.
C. T. Jester, Shell Solar Industries
J. Kalejs, RWE Schott Solar
Khattak, Crystal Systems, Inc.

The rump session preceded the main workshop and was held on Sunday evening. It turned out to be a big attraction**.** Nearly all workshop attendees participated in this session. It began with brief presentations by each panelist expressing their views of R&D issues for the PV industry and the potential solutions they perceive. The list of the issues presented is given below.

- Terry Jester presented results of detailed experiments, which tracked the minority-carrier lifetime through various process steps. These results showed:

  — Minority-carrier lifetime is a meaningful measurement that reflects the quality of the material for Shell Solar's single-crystal CZ Si.
  — Cell efficiencies correlate with as-grown ingot lifetimes, which in turn correlate with after-oxidation lifetimes.
  — Ingots grown by two larger pullers have shorter lifetimes than those obtained using smaller pullers. The two types of pullers (CG3000– 6000) are different in physical structures, in feedstock materials, and in pulling processes. Cell efficiency distributions exhibit two tails—one corresponds to low V and the other to low I_{sc}. Beads, remelt, and low growth rate are not the causes of lower lifetime. Experiments are now in progress to narrow down the responsible factors.
  — A cost cutting parameter can be Ar flow.

- Tim Bruton speculated on the future of high efficiency cells.

  — Improvement in the cell efficiency is a primary parameter for cost reduction.
  — 20% cells are routinely fabricated in the laboratory on single-crystal Si (sc-Si) using manufacturable processes; perhaps 18% cells can soon be realized in the laboratory for multicrystalline Si (mc-Si). However, commercial production of these devices could take some time. It is not clear what is beyond the 20% sc-Si or 18% mc-Si cells.

- Jack Hanoka addressed string ribbon issues.

  — Hopes to make ~18% cells on Evergreen ribbons in 3-5 year time frame.
  — H passivation is a panacea. Understanding role of H-passivation is crucial. Hydrogen passivation followed by rapid quenching would help, as it appears to be highly effective in passivating defects. Quenching is essential to hold H in active state.
  — Has some concern of Si supply; lower cost silicon needed.
  — Thinner Si and thin ribbon handling are near-future issues.

- Juris Kalejs emphasized the need for "clean" Si for high-efficiency cells.

  — Low-cost Si does not mean high efficiency.
  — Due to the large amounts of impurities present in solar grade Si, 18%-20% cell efficiency is generally incompatible with mc-Si. In an EFG ribbon, only some local regions of the cell may have efficiency reaching these values. They use semiconductor grade feedstock for high efficiency ribbons.
  — They draw 30 cylinders (150 Kg melt) from one crucible.
  — He thinks thickness must go down and width must go up. To accommodate current thickness and width, they grow at 0.75 ips. This yields about 14% average efficiency.

- Chandra Khattak emphasized the need for improving solar cell yield.

  — The future of PV is in crystalline Si. However, there is need for low-cost and high-quality processes, because cell yields are crucial. Technology for producing low-cost, high-quality mc-Si seems to be available.
  — Current solar cell costs are primarily determined by the yield, not by processing or efficiency.

Salient items from general discussions:

- In general, the quality of current mc-Si materials is much higher than it was few years back. For example, EFG ribbons exhibit minority-carrier lifetimes of 4-5 μs as-grown and 80-100 μs after cell fabrication.

- The laboratory version of 20% cells is expected to be made in the near future. Improving CZ cells from the current range of 15%-17% to 20% in production could be a real challenge. Hydrogen passivation may help.

- Minority-carrier lifetime of CZ-Si for solar cells is believed to be lower than semiconductor CZ Si because it is pulled faster, uses low-cost crucible, low Ar flow, and has lower-grade feedstock. Backside cells, at 20%, need 1 ms lifetime, front side cells do okay with 250 μs. Silicon seems to need << 1E11 metallic impurities for 18%.

- There was a general consensus that n-type substrates should be tested for solar cell fabrication. 20% cells used n-type Si for which it is easier to deal with defects. But n-type materials have other problems, e.g., contacts, etc. Sanyo use n-type material, but what is the increased cost?

- 20% cells could be the end of the line product for thick cells using CZ and FZ Si materials. Need thin Si to go beyond 20%.

- PV companies are seemingly not coming together with universities in collaborations and exchanging formation, though there are examples of one-on-one contacts. Contacts should go beyond this Workshop and beyond one-on-one.

- It is generally believed that metallization inks (Al and Ag pastes) are highly impure. Higher purity is needed from these pastes. However, there is no evidence that purity of pastes is a big issue for contamination.

- B-O pairing is responsible for light degradation of cells. How about Ga-doped Si and/or high resistivity (~5 ohm-cm) Si?

- As of now, 20% cells produce 17% modules. How to lead to ~20% modules?

- Light degradation in CZ. What is the cost of Ga doping?

- U. S. funding seems to be the inverse of the world trend: crystalline Si is barely funded, whereas funding is more abundant for other efforts. Funds could be leveraged if some of it can be converted into $25k-student scholarships.

Session 2:Crystal Growth

Discussion Leader: G. Rozgonyi, North Carolina State University

Discussions were directed toward each growth process discussed in the oral presentations.

On sliver cells:

- There was some general concern that Sliver cells were hard to handle; but, it was pointed out that: the sliver cells are made from a FZ Si substrate, which has very little to no residual stress. Also, it is very thin (~50-70 micrometers), hence it is highly elastic. Consequently, they are fairly easy to handle.

- Because sliver cells have only been made from FZ Si, it is not yet known whether there will be a difference from those made using CZ Si.

On modeling of CZ and FZ Si growth:

- Modeling of dopant incorporation in CZ Si growth is difficult, and, hence, it is also difficult to predict Ga distribution. But it is relatively easy to model dopant distribution in FZ Si growth.

On string ribbon growth:

- The fundamental limit for ribbon width is residual strain, which increases with the ribbon width.

- Thermal gradient is crucial for string ribbon growth.

- It is unknown whether nitrogen can block dislocation generation.

- Surface films formed in growth ambient are detrimental to ribbon materials.

Session 3: Impurities, Defects, and Gettering

Discussion leader: D. Schroder, Arizona State University

- The upper limit for the efficiency of Si solar cells is about 25%. The most important factor limiting the efficiency is the surface recombination velocity, which is difficult to improve on the front contact cells. It is also difficult to make backside contacts for still higher efficiency cells.

- Degradation of minority-carrier lifetime by light (LID) in sc-Si, is due to formation of B-O pairs or complexes. The effect of B-O complexes on cell efficiency is not well known. There are no indications of being able to control B-O complexes, making the only viable options for eliminating LID either Ga-doping to get p-type Si or using n-type Si.

- Although impurity gettering is normally associated only with mcSi cell fabrication, high-efficiency sc-Si cells might also need gettering.

- Multicrystalline Si has low bulk lifetimes because of impurities and defects. Hence, cell fabrication includes gettering and H passivation. However, "bad" regions do not respond to gettering, due to difficulties of dissolving precipitates for thermodynamic and chemical reasons.

- Because solar cells are bulk devices, gettering for solar cells is a more demanding scheme than in ICs. So far only the external methods of P-gettering and Al-gettering are seemingly useful. It may be that internal gettering can be used to localize metallic impurities into an inactive state. For high-quality Si and clean processing, there is no need for gettering.

- H passivation is not well understood, including its stability at the defect, the role of Al in enhancing passivation, what is passivated, and whether it can improve bad regions in mc-Si.

- The characterization needs include lifetime measurements, DLTS, EBIC, MBIC, LBIC, and PL

- What about shorts and shunts?

Session 4: High-Efficiency Cells

Discussion Leaders: A. Gabor, Evergreen Solar, Inc.
V. Yelundur, Georgia Institute of Technology

- Attaining high-efficiency cells is only a part of the goal to achieve high-efficiency modules at a reasonable cost.

- High-efficiency cell fabrication generally involves more expensive cell design processing facilities and higher-quality feedstock. An intelligent compromise may be reached for a cost-efficiency compromise.

- Can high efficiency cells be realized via processing and cell design changes? Simulations indicate mc-Si can be made into ~19% cells from the usual ~14% normal cells by a variety of improvements: metallization, reduced line width, Al gettering-backside field, high sheet resistance emitter or selective emitter, etc. The question is, how practical?

Session 5: Processing Issues in the Future

Discussion Leaders: Mohan Narayanan, BP Solar
Ron Sinton, Sinton Consulting, Inc.

Processing issues in the solar cell manufacturing industry are still largely developed within industry. Although more vendors are developing equipment and processes for the industry, incorporation of these processes into the factory usually involves collaboration between the vendor and the solar cell production line, sometimes for several years to sort things out. The time required for this collaboration is getting shorter with time, but, at present, there are not yet turnkey process solutions available to industry.

There was some discussion of the need for an analog to the SEMATECH model for equipment development. Should NREL have increased internal activities in crystalline silicon to support this topic that accounts for nearly the entire PV industry? Should a university set up a "Center for Solar Cell Manufacturing R&D"?

There are several topics where nearly all solar cell manufacturers have a common interest. This includes thin wafer processing. The need to process thin wafers is now seen as a necessity, not a novelty. There is much interest in developing a generic understanding of wafer handling, how to mimimize and manage microcracks, etc. Improved light trapping for ribbons and multi-crystalline materials is another common requirement as we trend toward thin solar cells.

There is still a need for the incorporation of better statistical process control within the manufacturing lines. This requires better SPC tools. When asked what was required for the cells and processes envisioned for the future, two candidates emerged. The first was a tool for determining back surface recombination velocity. It is thought that the efficiency for thin wafers will be surface-recombination limited. The second class of tools would be anything that would help to improve mechanical yield. The dominant yield problem is not electrical yield, it is mechanical yield.

Session 7: Automation/Equipment

Discussion Leaders: Julio Bragagnolo, NPC America Corporation
Ralf Preu, Fraunhofer ISE

This session was held to get a feedback from the audience pertaining to major design issues for the equipment used in the PV industry. Of particular interest were the areas of wafer handling, throughput, machine downtime, maintenance, and in-line testing capabilities. The questions posed to the audience were:

1. What are realistic industry targets for wafer breakage, throughput, and downtime?

2. What are the major sources of downtime in current manufacturing equipment?

3. What key in-line testing capabilities are needed for current cell production?

4. What processes would benefit most from additional automation, and at what processing speed?

5. Is there a good, high-speed test to detect cracks before lamination?

6. What, if any, are the advantages of ELH light sources vs. Xenon sources in cell and module testing?

7. For in-line cell factories, what are the key buffer issues to resolve? Is there a simulation model that is commonly used in the industry to determine the optimum buffer configuration?

Salient results of the discussion:

- It was generally felt that wafer breakage is a dominant issue for the PV industry. Incorporating automation of wafer transport could reduce a fraction of wafer breakage. The other source of wafer breakage is wafer processing itself. In general, minimizing or eliminating microcracks on wafers may be the most effective way to enhance yield. A process yield exceeding 90% must be attained.

- Typically a batch-processing machine must be able to handle about 1000 wafers/hour.

- Every major manufacturing facility has some degree of automation and each company has independently developed automation tools. Automated wafer pick-up and sorting are now highly prevalent. Stringing and encapsulation will benefit the most from automation.

- At the present time, there is no high-speed technique for crack detection.

Session 8: Thin Si Solar Cells

Discussion Leaders: Bolko von Roedern, NREL and Tihu Wang, NREL

This session started with a goal of determining if there was a consensus in the audience regarding the approach(es) the PV industry will follow in the transition to thinner cells (including thin-film Si solar cells). Discussion leaders also posed several questions to the workshop attendees to assess the status of technology needed for fabrication of efficient thin Si cells. They include:

- Are there any preferred approaches that might make an early entrance to thin cell manufacturing? For example, could thinner ribbons, lift-off films, or monolithic interconnected thin films precede other approaches?

  It was clear that industry is on already a path to reducing cell thickness. This effort is being dampened by excessive wafer breakage of thinner wafers during device processing. Industry is already convinced that thinner wafers will yield higher efficiencies and diminish demands on feedstock. However, production of thin-film cells will take several more years.

- Is there a distinct direction for fabrication of thin-film Si? For example, does the community favor high-T or low-T deposition and processing approaches? Is there any hope of finding viable approaches for films with intermediate grain sizes ("valley of death")?

There does not seem to be a well-defined direction to thin-film Si solar cells. Many approaches may survive.

- Has Si lived up to its promise?

  — A promoted strength for Si has been that this semiconductor is the best-understood material. However, there is lot more to learn before each cell process step is optimized (using highly specialized approaches).
  — Do we understand the physics (or why we are doing what we are doing during cell processing)?
  — Are "defects" really limiting cell performance (or are their critical defect densities for specific approaches)?

It was generally felt that industry is keen on deriving the advantages of thinner cells, but it is clear that the production of thin Si cells will offer major challenges. Cell yield is the foremost problem for thinner wafers. Perhaps there will be a gradual (stepwise) reduction in the cell thickness.

Thin cells will alleviate some problems associated with material-quality variation in the industry, but they will require high-quality surface passivation.

There are no clear-cut answers as to what approaches will be the winner(s) in thin-film solar cell production. Although a great deal of progress has been made toward understanding the role of

impurities and defects in Si solar cells, with concomitant increase in the average cell/module efficiencies, new challenges emerge as we achieve higher cell efficiencies.

Wrap-Up Session

Moderator: Dick Swanson, SunPower Corp.

The market expansion is driving a new stage of innovation in crystalline silicon solar cells with advances in both cell efficiency and cost. These advances are across the board, with some companies focused on low-cost silicon (ribbons, "sliver" solar cells) and others optimizing the cost and efficiency of multicrystalline solar cells. New entries into the high-efficiency area include cost-effective backside-contact solar cells, HIT cells, and OECO cells in addition to the well-established buried-contact solar cells.

It was evident at this workshop that the market expansion has accelerated the incorporation of new research and technology into solar cell manufacture. Major changes in the basic production process are being incorporated into new lines and refitted into older lines. For example, the nearly universal adoption of plasma silicon nitride into the process has created a demand for research results that will optimize the surface passivation qualities, bulk passivation, and contact-firing optimization for this material. The research shows that the details of this implementation will have major effects on the efficiencies, and that the understanding of the available parameter space is still at an early stage. The promise of additional gains from this optimization is clear from both industrial and laboratory results. This was just one example progress in the cost and efficiency optimization within industry.

In the larger view, the cost of crystalline silicon modules continues to decrease down an experience curve with increased production. This is shown in Fig. 1.

Several factors have driven the cost reductions evident in Fig. 1. These include:

- Wire saws: now < \$0.25/W
- Poly silicon price: \$300/kg → \$30/kg
- Larger wafers: 3" → 6"
- Thinner wafers: 15 mil → 10 mil
- Improved efficiency: 10% → 16%
- Volume manufacturing: 1 MW → 100 MW
- Increased automation: none → some
- Improved manufacturing processes.

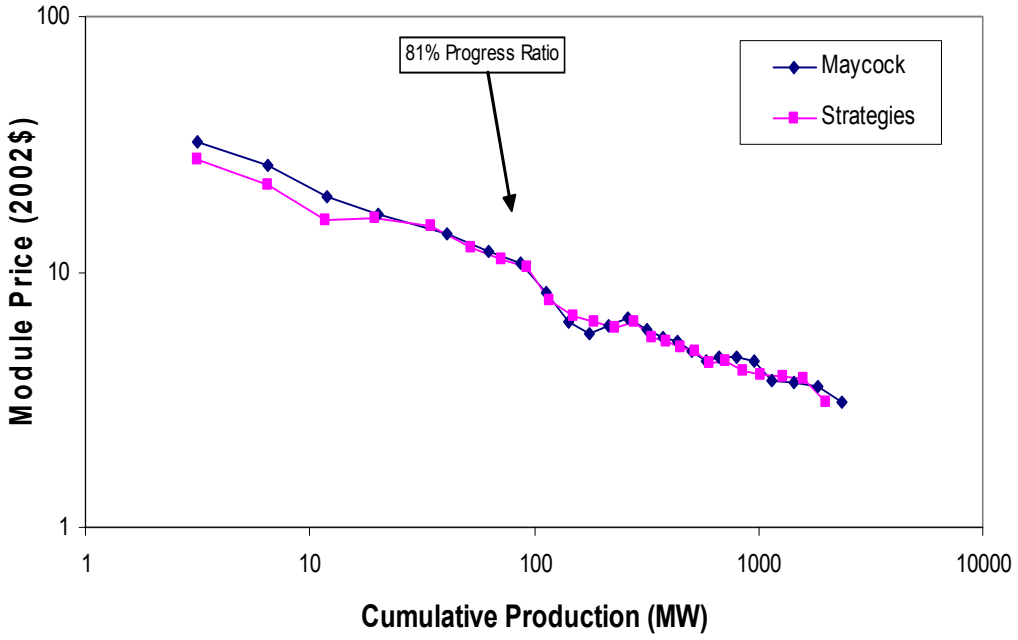

Fig. 1. An experience curve for PV module manufacturing. No asymptotic limit to the module price is visible at this time. This continuing progress presents a difficult moving target for the significant market introduction of new thin-film technologies.

Some results from the participant survey at the 2002 Workshop were referenced, and compared to results and predictions from the various presentations at the 2003 Workshop to benchmark continuing progress in these areas.

Relative to the survey, several speakers presented predictions or plans for the future efficiency of their cells. These are shown in Fig. 2, relative to the survey predictions. Several approaches are being pursued to result in marketable products. The SunPower result aims to primarily maximize watts while keeping cost within reason. The Fath and Tsuo predictions are for pursuing evolutionary cost and efficiency improvements within the low-cost cell fabrication processes that dominate the industry today.

Similarly, the trend towards thinner wafers in being pursued industry wide. An example of the expectation of industry members relative to last year's survey results is shown in Fig. 3.

Suggestions for potential invited papers for the 14th Workshop were discussed. One topic that surfaced at virtually every discussion session in the workshop was the handling of thin wafers. Although there are still numerous technologies in crystalline silicon of all sizes and shapes using float-zone wafers, CZ wafers, multicrystalline wafers, and ribbons, there exists a strong common need in every case for high-yield as we trend toward thin wafers for both cost and efficiency. Advances presented at the workshop will be widely appreciated. There was enthusiasm for the talk of Rob Ritchie at this workshop, and demand for follow-up work and discussion. A presentation on specific processes for handling wafers would be good.

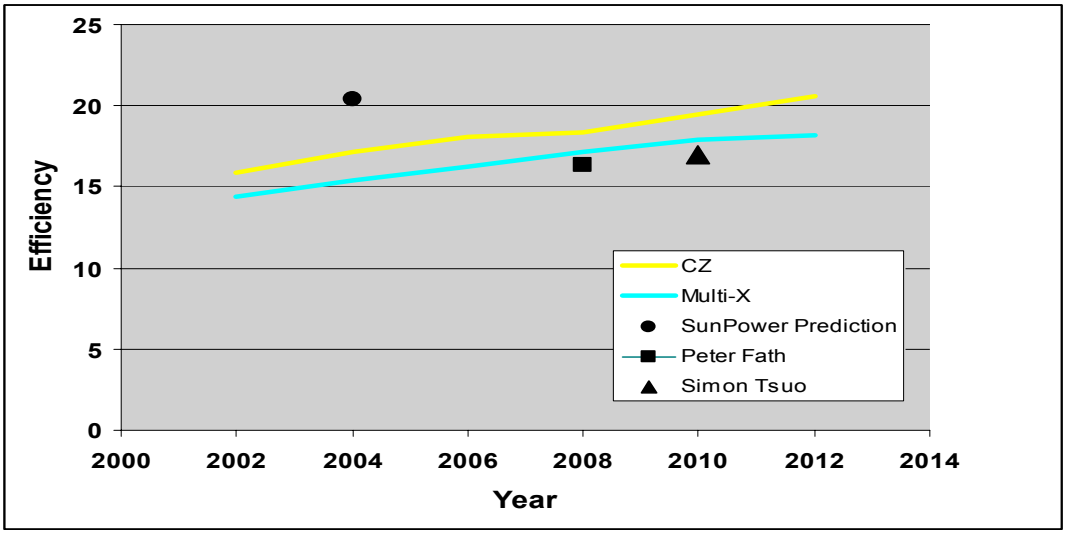

Fig. 2. The results of a 2002 survey at the Workshop for the expected trend in efficiency for CZ (top curve) and Multi-X (bottom curve). SunPower is currently installing a line to produce cells with efficiency over 20%. In a survey by Peter Fath, it was found that industry widely anticipates product averaging 16% by 2008. Simon Tsuo sees 17% by 2010.

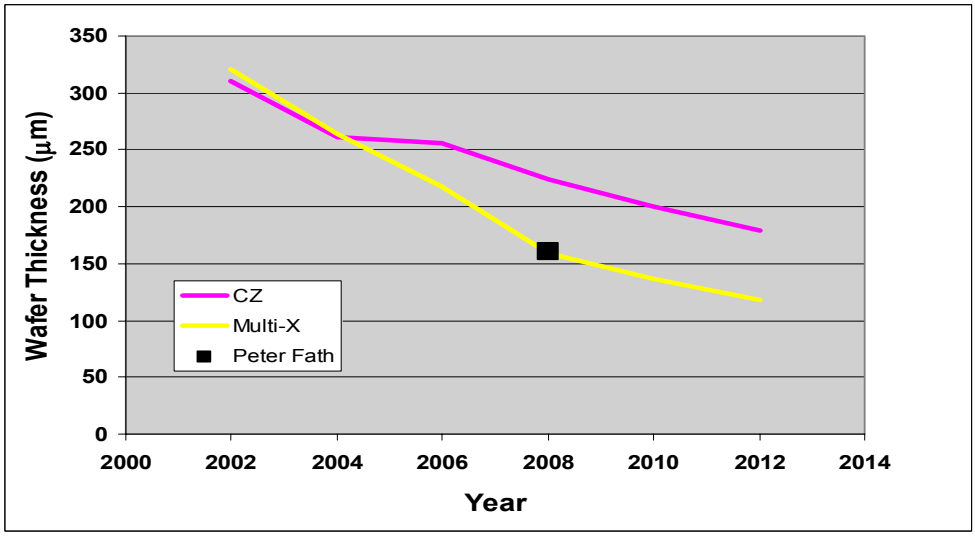

Fig. 3. The predictions from the 2002 workshop survey concerning wafer thickness in solar cell production lines. Another data point, based on an industry survey by Peter Fath, is shown for reference.

A talk on applied diagnostics was requested, specifically addressing new diagnostics that were being applied within industry or are ready for application in the production environment.

This workshop featured a talk by a representative from Wacker emphasizing the sophistication of the modeling tools used in the integrated-circuit industry. It was pointed out that further topics in this area, the sophisticated use of modeling in crystal growth, would be appreciated at future workshops.

There is a great interest in the experimental work being done on hydrogen passivation in silicon. We should have an update on this work.

At this 13th Workshop, there was some disagreement in the predictions of the price of silicon. The workshop should continue to focus on ways to reduce the sensitivity of the industry to this price by featuring advances in solar cell and process design that minimize silicon use. One topic that needs a review is the potential for cost-effective epitaxial silicon.

One interesting point that emerged from the presentations and discussions in the workshop was that there is a huge discrepancy between the chemical concentrations of "contaminants" in silicon and the concentration of harmful electrically active defects. For example, the light-degradation in silicon is strongly linked to both the boron and oxygen concentrations. However, with boron at 2 x 10^{16} cm^{-3} and oxygen at 6 x 10^{17}, they give rise to a defect concentration with a concentration of less than 1 x 10^{11} cm^{-3}, but still depend critically on the oxygen and boron concentrations. Similarly, transition metals are found in most of the solar silicon materials at concentrations orders of magnitude higher than the active defect concentrations. We need to understand how to manipulate the chemical state of defects to our advantage. Clearly we are already doing this to some degree, but the understanding is lagging the empirical recipes in this area.

There was general agreement that the very compact schedule was preferred for industrial participants so they are not "out of the office" for the entire week. However, the schedule seemed a bit too intense this year, with time tightly scheduled from 7.00 a.m. to 9.00 p.m. The rump session on Sunday night was quite successful at adding technical content and bringing everyone together for a bit more interaction. It was suggested that the schedule could be relaxed a bit if we took advantage of the fact that most people arrived from out of town on Saturday for optimum airline pricing. We could start on Sunday afternoon and then loosen up the schedule on Monday and Tuesday.

Talks should be optimized to leave adequate time for discussion. Speakers should be told ahead of time to prepare talks to fill less than the entire time slot.

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